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EXAMINER	
LUU, CUONG V	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/044,217	ZEIDMAN, ROBERT M.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *64-70 and 72-101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *64-70 and 72-101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/7/2010 has been entered.

DETAILED ACTION

Claims 64-70 and 72-101 are pending. Claims 86-101 have been added. Claims 1-63 and 71 have been canceled. Claims 64-70 and 72-101 have been examined. Claims 64-70 and 72-101 have been rejected.

Response to Arguments

Applicant's arguments with respect to claims 64-70 and 72-85 have been considered but are moot in view of the new ground(s) of rejection. The Applicant arguments centers on a point that the AAPA and Evans in combination do not teach in claim 64 the feature a computer receiving one or more digital data packets at a first transmission rate from [a] computer peripheral device, and "sending data contained in the received digital data packets to [an] emulator at a second transmission rate over a computer peripheral interface coupled to the computer system, wherein the second transmission rate is slower than the first transmission rate," and wherein the emulator is "configured to emulate a design of an integrated circuit designed to communicate bidirectionally with the computer peripheral device. Evans in col. 8 line 55 through col. 9 line 3, col. 9 lines 21-28, and col. 10 lines 5-24 teaches a computer coupled to an emulator and connected with another computer through a

network via a peripheral device. In these lines Evans teaches a method for verifying a multi-component electronic design in which one component runs at speed slower than the rest of the components by implementing higher speed components on an emulator board and simulating the slow speed component on a computer, wherein the simulation computer and emulator board are connected via a host computer wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a simulated component on a computer). Evans, therefore, teaches a computer is used to receive data at a higher speed source, the emulator, to send them to a slower speed sink, a computer via a peripheral device and vice versa. The computer 114 is used as an interface for speed difference. Hence, it would be obvious for one of ordinary skill in the art to use the same system connection to implement the communication in the case that the emulator's speed is now slower than the peripheral device since the communication is still receiving data from a high speed device to send to a slower speed device. Evans, however, does not teach store the digital data packets in a memory buffer and retrieve the digital data packets from the memory buffer. However, Gagne teaches store the digital data packets in a memory buffer (col. 1 lines 60-68 and col. 2 lines 1-2) and retrieve the digital data packets from the memory buffer (col. 1 lines 60-68 and col. 2 lines 1-2). It would have been obvious to one of ordinary skill in the art to combine the teachings of the Evans and Gagne. Gagne's teachings would have provided buffers dedicated to different destinations (Gagne, col. 1 lines 60-68 and col. 2 lines 1-2). Claim 64, therefore, is rejected. For the same arguments, the Applicant requested withdrawals of 35 USC 103 rejections of claims 73 and 81. Claims 73 and 81 are rejected for the same reasons discussed above.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 87-91 are rejected under 35 U.S.C. 101.

1. Claims 87-91 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter, program per se. The limitations claim a program performing tasks of a method.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 87-91 are rejected under 35 USC 112, 2nd paragraph.

2. As per claims 65, 90, 94, and 99 the term "suitable" renders the claim indefinite. It is not clear how it is "suitable" for transmission.

3. Regarding claim 87, the phrases "the program storing", "the program retrieving", and the "program transmitting" render the claim indefinite because it is unclear how a program can perform a task by itself. A program can only be executed on a CPU to perform task.

4. Regarding claim 89, the phrases "the program keeping a record" renders the claim indefinite because it is unclear how a program can perform a task by itself. A program can only be executed on a CPU to perform task.

5. Claims 88-91 inherit the defects of claim 87.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 64-65, 67-69, 72-73, 75-77, 80-81, 83-88, 90, 92-94, and 97-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. (U.S. Pat. 6,279,146 B1) in view of the Gagne et al. (U.S. Patent 5303347).

6. As per claim 64, the Evan teaches system, comprising:

at least one processor (col. 8 lines 50-51); and

a memory (col. 8 lines 50-51. A computer inherits a memory);

wherein the computer system is configured to couple to an emulator, wherein the emulator is configured to emulate an integrated circuit designed to communicate bidirectionally with a computer peripheral device (col. 8 line 55 through col. 9 line 3. The emulator 60 communicates bidirectionally with a computer 118, which is connected with computer 114 via a computer peripheral device. This teaching reads onto this limitation);

wherein the memory has computer instructions stored thereon that are executable by the at least one processor to cause the computer system to:

receive one or more digital data packets at a first transmission rate from the computer peripheral device (col. 9 lines 21-28);

send data contained in the buffered data packets to the emulator at a second transmission rate over a computer peripheral interface coupled to the computer system, (col. 9 lines 21-28).

but does not teach:

store the digital data packets in a memory buffer;

retrieve the digital data packets from the memory buffer; and

wherein the second transmission rate is slower than the first transmission rate.

Gagne teaches:

store the digital data packets in a memory buffer (col. 1 lines 60-68 and col. 2 lines 1-2);

retrieve the digital data packets from the memory buffer (col. 1 lines 60-68 and col. 2 lines 1-2);

Evans teaches the first transmission rate is slower than the second transmission rate (col. 10 lines 5-24. In these lines Evans teaches a method for verifying a multi-component electronic design in which one component runs at speed slower than the rest of the components by implementing higher speed components on an emulator board and simulating the slow speed component on a computer, wherein the simulation computer and emulator board are connected via a host computer wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a simulated component on a computer). Evans, therefore, teaches a computer is

used to receive data at a higher speed source, the emulator, to send them to a slower speed sink, a computer via a peripheral device and vice versa. The computer 114 is used as an interface for speed difference. Hence, it would be obvious for one of ordinary skill in the art to use the same system connection to implement the communication in the case that the emulator's speed is now slower than the peripheral device since the communication is still receiving data from a high speed device to send to a slower speed device).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the Evans and Gagne. Gagne's teachings would have provided buffers dedicated to different destinations (Gagne, col. 1 lines 60-68 and col. 2 lines 1-2).

7. As per claim 65, Evans teaches wherein the instructions are executable to cause the computer system to modify data in the received one or more digital data packets to make the data suitable for transmission to the emulator (col. 9 lines 17-28).

8. As per claim 67, As discussed in claim 64, it would be obvious for one of ordinary skill in the art to use the same system connection to implement the communication in the case that the emulator's speed is now slower than the peripheral device since the communication is still receiving data from a high speed device to send to a slower speed device. This discussed obviousness reads onto this limitation of the emulator is incapable of receiving and processing data sent to the emulator at the first transmission rate.

9. As per claim 68, Evans teaches wherein the emulator is implemented, at least in part, using field programmable gate arrays (col. 9 lines 60-65); and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit (col. 9 lines 60-65), wherein the design allows bidirectional communication with the computer peripheral device (already discussed in claim 64).

10. As per claim 69, Evans teaches the computer peripheral interface is a network connection (col. 8 lines 44-49. The PCI connection between the emulator having controller 112 with computer 114 is considered a network connection); and

wherein the instructions are executable to cause the computer system to repackage data from the stored digital data packets (col. 9 lines 17-28);

11. As per claim 72, Gagne teaches the received one or more digital data packets are variable in size (col. 1 lines 60-66).

12. As per claim 73, these limitations have already been discussed in claim 64. They are, therefore, rejected for the same reasons.

13. As per claim 75, Evans teaches:

the first computer repackaging data from the buffered data packets (col. 9 lines 17-28);

wherein the repackaged data is the data sent from the first computer to the emulator (col. 9 lines 17-28).

14. As per claim 76, this limitation has been discussed in claim 68. It is, therefore, rejected for the same reasons.

15. As per claim 77, Evans teaches the emulator sending data corresponding to the received and processed data to a second computer (col. 9 lines 17-28).

16. As per claim 80, these limitations have already been discussed in claim 68. They are, therefore, rejected for the same reasons.

17. As per claim 81, these limitations have already been discussed in claim 64. They are, therefore, rejected for the same reasons.

18. As per claim 83, Evans teaches the computer peripheral device is a network device and wherein the received one or more digital data packets are transmitted from the network device via a network connection according to a network communications protocol (col. 9 lines 59-65. In these lines Evans teaches the 2 computers connected via a LAN, so it reads onto this limitation).

19. As per claim 84, these limitations have already been discussed in claim 69. They are, therefore, rejected for the same reasons.

20. As per claim 85, these limitations have already been discussed in claim 67. They are, therefore, rejected for the same reasons.

21. As per claim 86, Evans teaches the computer peripheral device is coupled to a different computer system, wherein the different computer system is configured to send data from the

computer peripheral device via a network interface, and wherein the network interface is the computer peripheral interface (col. 9 lines 59-65. In these lines Evans teaches the 2 computers connected via a LAN, so it reads onto this limitation).

22. As per claim 87, Evans teaches a method comprising:

receiving digital data from a circuit emulator at a program running on at least one processor of a computer, wherein the digital data is received at a first transmission rate, and wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a computer peripheral device (col. 8 line 55 through col. 9 line 3. The emulator 60 communicates bidirectionally with a computer 118, which is connected with computer 114 via a computer peripheral device. The computer 114 has a program to control the communication back and forth between the emulator and other computers. These teachings read onto this limitation);

but does not teach:

the program storing the received data in a memory of the computer ;

the program retrieving the stored data from the memory; and

the program transmitting the retrieved data to the computer peripheral device at a second transmission rate over a computer peripheral interface coupled to the computer, wherein the first transmission rate is slower than the second transmission rate.

Gagne teaches.

the program storing the received data in a memory of the computer col. 1 lines 60-68 and col. 2 lines 1-2);

the program retrieving the stored data from the memory col. 1 lines 60-68 and col. 2 lines 1-2); and

Evans teaches the second transmission rate is slower than the first transmission rate (col. 10 lines 5-24. In these lines Evans teaches a method for verifying a multi-component electronic design in which one component runs at speed slower than the rest of the components by implementing higher speed components on an emulator board and simulating the slow speed component on a computer, wherein the simulation computer and emulator board are connected via a host computer wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a simulated component on a computer). Evans, therefore, teaches a computer is used to receive data at a higher speed source, the emulator, to send them to a slower speed sink, a computer via a peripheral device and vice versa. The computer 114 is used as an interface for speed difference. Hence, it would be obvious for one of ordinary skill in the art to use the same system connection to implement the communication in the case that the emulator's speed is now slower than the peripheral device since the communication is still receiving data from a high speed device to send to a slower speed device).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the Evans and Gagne. Gagne's teachings would have provided buffers dedicated to different destinations (Gagne, col. 1 lines 60-68 and col. 2 lines 1-2).

23. As per claim 88, these limitations have already been discussed in claim 67. They are, therefore, rejected for the same reasons.

24. As per claim 90, Evans teaches the program modifying the received data from the circuit emulator to make the data suitable for transmission to the computer peripheral device (col. 9 lines 17-28).

25. As per claim 92, these limitations have already been discussed in claim 87. They are, therefore, rejected for the same reasons.

26. As per claim 93, these limitations have already been discussed in claim 88. They are, therefore, rejected for the same reasons.

27. As per claim 94, these limitations have already been discussed in claim 90. They are, therefore, rejected for the same reasons.

28. As per claim 97, these limitations have already been discussed in claim 87. They are, therefore, rejected for the same reasons.

29. As per claim 98, these limitations have already been discussed in claim 88. They are, therefore, rejected for the same reasons.).

30. As per claim 99, these limitations have already been discussed in claim 90. They are, therefore, rejected for the same reasons.

Claims 74, 78-79, and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. in view Gagne et al. as applied to claim 73 and 81 above and further in view of the AAPA.

31. As per claim 74, the AAPA teaches the data sent to the second computer is usable to debug the design of the integrated circuit (p. 1 lines 10-12); and

Evans teaches the interface is a network connection (already discussed in claim 69).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the Evans, Gagne, and the AAPA. The AAPA's teachings would have helped an emulator to be connected to a network for debugging (the AAPA, specification p. 1 lines 10-20).

32. As per claim 78, the AAPA teaches the emulator is configured to emulate a network interface card of the second computer (p. 1 lines 23-26. In these lines the AAPA teaches the emulator process data and transmit data. This teaching is interpreted as transmitting data to a second computer after the emulator having a network interface receiving data, so it should read onto this limitation); wherein the integrated circuit is designed to be a component of the network interface card; and

wherein the first transmission rate is a data rate of an Ethernet network (the AAPA, specification p.1 lines 18-20).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the Evans, Gagne, and the AAPA. The AAPA's teachings would have helped an emulator to be connected to a network for debugging (the AAPA, specification p. 1 lines 10-20).

33. As per claim 79, Gagne teaches the computer is configured to, for each incoming data packet:

examining that data packet (col. 1 line 60 through col. 2 line 2. In these lines Gagne teaches receiving data and put them in proper buffers for different destination. This teaching implies that data packets are examined);

determine if that data packet is addressed to a destination (col. 1 line 60 through col. 2 line 2. In these lines Gagne teaches receiving data and put them in proper buffers for different destination. This teaching reads onto this limitation); and

if that data packet is addressed to a destination, buffering that data packet and sending data contained in the buffered packet to the destination (col. 1 line 60 through col. 2 line 2. In these lines Gagne teaches receiving data and put them in proper buffers for different destination. This teaching reads onto this limitation).

The AAPA teaches the emulator is configured to emulate a network interface card (specification p. 1 lines 21-26).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Evans, Gagne, and the AAPA. The combination of these teachings would have provided a method to direct data a specific destination, in this case an emulator, which emulates a network interface card (the AAPA, specification p. 1 lines 21-26).

34. As per claim 82, these limitations have already been discussed in claim 79. They are, therefore, rejected for the same reasons.

Claims 70, 95, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. in view of Gagne et al. as applied to claim 65, 92, and 97 above, and further in view of Watanabe et al (U.S. Pat. 5761486).

35. As per claim 70, Evans and Gagne do not teach the second computer is further configured to log data corresponding to received data and/or sent data in a log file.

However, Watanabe teaches keeping a record of communicated data from source to destination (col. 6 lines 18-23).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Evans, Gagne, and Watanabe. Watanabe's teachings would have provided designers information of the emulation in order to analyze and evaluate the emulation (col. 3 lines 43-51).

36. As per claim 95, these limitations have already been discussed in claim 70. They are, therefore, rejected for the same reasons.

37. As per claim 100, these limitations have already been discussed in claim 89. They are, therefore, rejected for the same reasons.

Claims 66 and 91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. in view of Gagne et al. as applied to claims 65 and 87 above, and further in view of Chang et al. (U.S. Patent 6,047,387).

38. As per claim 66, Evans teaches the computer peripheral device is a network interface card (col. 8 line 55 through col. 9 line 3. In these lines, Evans teaches the computer 114 connected to computer 119 or 118 via a LAN. This implies the computer peripheral device is a network interface card); but does not teach wherein the instructions are executable as a multi-threaded program.

Chang teaches a thread for receiving data and a thread for transmitting data (col. 4 lines 10-19).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the AAPA and Chang. Chang's teaching would have controlled the data transmission to or from a simulation module (col. 4 lines 10-21) that in combination with data comparison with intended results to assess the precision of return signals to achieve necessary functional testing (col. 3 lines 1-7).

39. As per claim 91, Evans teaches wherein the computer peripheral device is a network interface device (col. 9 lines 59-65. In these lines Evans teaches the 2 computers connected via a LAN, so it reads onto this limitation).

Evans and Gagne do not teach said receiving data from the circuit emulator is executed in a first thread, and said transmitting the data received from the circuit emulator is executed in a second thread.

Chang teaches a thread for receiving data and a thread for transmitting data (col. 4 lines 10-19).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Evans, Gagne, and Chang. Chang's teaching would have controlled the data transmission to or from a simulation module (col. 4 lines 10-21) that in combination with data comparison

with intended results to assess the precision of return signals to achieve necessary functional testing (col. 3 lines 1-7).

Claim 89 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. in view of Gagne et al. as applied to claim 65, 87, 92, and 97 above, and further in view of Watanabe et al (U.S. Pat. 5761486) and the AAPA.

40. As per claim 89, Evans and Gagne do not teach the program keeping a record of the data received from the circuit emulator, wherein the received data is usable to optimize and/or debug a design of the integrated circuit. Watanabe teaches keeping a record of the data received (col. 6 lines 18-23) and the AAPA teaches the data sent to the second computer is usable to debug the design of the integrated circuit (p. 1 lines 10-12).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Evans, Gagne, Watanabe, and the AAPA. Watanabe's and the AAPA's teachings would have provided designers information of the emulation in order to analyze and evaluate the emulation (Watanabe, col. 3 lines 43-51) and helped an emulator to be connected to a network for debugging (the AAPA, specification p. 1 lines 10-20)

Claim 96 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans in view of Gagne et al. as applied to claims 92 and 97 above, and further in view of Chu et al (ACM, 0-89791-089-3/83/0300-0170, 1983).

41. As per claim 96, Gagne and Evan do not teach the operations further include recording the throughput of the transmitted data.

However, Chu et al teach this feature (p. 171, col. 2, paragraph 5, lines 1-6).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Gagne, Evan, and Chu. Chu's teaching of recording the throughput of the data packets would have provided designers performance statistics of devices under simulation to make decisions about modification, re-design, or adjustment regarding the those devices.

42. As per claim 101, these limitations have already been discussed in claim 96. They are, therefore, rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong V Luu/

Examiner, Art Unit 2128

/Hugh Jones/

Primary Examiner, Art Unit 2128